وازرة التعليم العالي والبحث العلمي جـــهاز

الإشـــراف والتقـــويم العلـمي

دائرة ضمان الجودة والاعتماد الأكاديمي

استمارة وصف البرنامج الاكاديمي للعام الدراسي ٢٠٢٤_٢٠٢٥ للكليات والمعاهد

الجامعة : جامعة شط العرب الاهلية

الكلية /المعهد : الكلية التقنية الهندسية

القسم العلمي : قسم هندسة تقنيات الأجهزة الطبية

تاريخ ملء الملف : 2025/8/4

التوقيع :

اسم رئيس القسم : د. هناء نبيل حسين

التاريخ : 2025/8/4

التوقيع :

اسم المعاون العلمي: أ.د. كامل حسين السوداني

التاريخ : 4/8/2025

الاستاذ الدكتور
كامل حسين السوداني
كيمياء تحليلية

الكلية التقنية الهندسية
اللجنة الامتحانية
هندسة تقنيات الاجهزة الطبية

دقق الملف من قبل

شعبة ضمان الجودة والأداء الجامعي

اسم مدير شعبة ضمان الجودة والأداء الجامعي: التاريخ

/ /

التوقيع

مصادقة السيد العميد

أ.م.د. مازن عبدالاله علوان

عميد الكلية التقنية الهندسية

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية					
Module Title	Digital Electronics			**Module Delivery**	
Module Type	Core			☒ **Theory** ☒ **Lecture** ☒ **Lab** ☐ **Tutorial** ☐ **Practical** ☐ **Seminar**	
Module Code	MIET2203				
ECTS Credits	5				
SWL (hr/sem)	125				
Module Level	2		**Semester of Delivery**	4	
Administering Department	MIET		**College**	EETC	
Module Leader	Saleem Lateef Mohammed		**e-mail**	saleem_lateef_mohammed@mtu.edu.iq	
Module Leader's Acad. Title	Professor		**Module Leader's Qualification**	M.Sc.	
Module Tutor	Ahmed Bashar Fakhri		**e-mail**	ahmed_bashar@mtu.edu.iq	
Peer Reviewer Name	Prof. Dr. Sadik Kamel Gharghan		**e-mail**	sadik.gharghan@mtu.edu.iq	
Scientific Committee Approval Date	8/11/2023		**Version Number**	1.0	

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	Electronics Circuits I (MIET2102)	**Semester**	S3
Co-requisites module		**Semester**	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Aims أهداف المادة الدراسية	1. To learn the basics of logical circuits which are used in computers. 2. To understand how the logical medical instrumentations to work 3. To program the logical medical instrumentations 4. To design the logical medical instrumentations 5. To learn how to use logical tables to perform the logical medical instrumentations 6. TO maintain the logical medical instrumentations 7. To suggest how to build modern the logical medical instrumentations.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	At ending of course, student will: 1-know the numbers systems, and conversion between them. 2-know binary codes. 3-design binary gates, and use Boolean algebra. 4-design and simplify the arithmetic circuits. 5- define Karnaugh maps. 6- know how flip-flops works RS, JK. 7- design flip-flops D, T. 8-define the work principles of counters and its types. 9-know the shift registers and types. 10-principles of decoders. 11-identify the Multiplexers and De-Multiplexers. 12-conversion of analog to digital circuits.
Indicative Contents المحتويات الإرشادية	**Numbers systems, Binary, Octal, Hexadecimal [4 H].** **Codes numbers [4 H].** **Arithmetic circuits [10 H].** **De Margan's theorems [4 H].** **Karnaugh map [8 H].** **Flip – Flop: RS, RST, JK, D, FF [8 H].** **Asynchronous counter and synchronous [10 H].** **Shift registers [10 H].** **Multiplexer, De multiplexer [4 H].** **Decoder [8 H].** **Analog conversion [4 H].**

Learning and Teaching Strategies استراتيجيات التعلم والتعليم	
Strategies	Type something like: The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering type of simple experiments involving some sampling activities that are interesting to the students.

Student Workload (SWL) الحمل الدراسي للطالب			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	79	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	5
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	46	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	3
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	125		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	2	10% (10)	3, 9	LO #1, 2, 4,11 and 12
	Assignments	2	10% (10)	3, 13	LO # 4, 5, 7 and 8
	Projects / Lab.	1	10% (10)	Continuous	
	Report	13	10% (10)	13	LO # 6, 8 and11
Summative assessment	**Midterm Exam**	2 hr	10% (10)	8	LO # 1-8
	Final Exam	2hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	**Number system: Binary numbers, Octal numbers, Hexadecimal numbers,**
Week 2	**Binary codes**
Week 3	**Logic gates, De Margan's theorems, Laws and theorem of Boolean algebra**
Week 4	**Arithmetic circuit, Simplifying logic circuits:**
Week 5	**fundamentals products, sum of products, algebraic simplification**
Week 6	**Truth table to Karnaugh map**
Week 7	**Flip – Flop: RS, RST, JK, D, FF**
Week 8	**Counters: Asynchronous counter**
Week 9	**Counters: synchronous counter**
Week 10	**Shift registers: Serial in -Serial out shift register** **Serial in -Parallel out shift register**
Week 11	**Shift registers: Bidirectional Shift Register**
Week 12	**Multiplexer and De multiplexer**
Week 13	**Decoder**
Week 14	**Digital to Analog converter**
Week 15	**Final Exam (Practical)**
Week 16	**Final Exam (Theoritical)**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	Lab 1: Logic Gates (NOT, AND)
Week 2	Lab 2: Logic Gates (OR, NAND, NOR)
Week 3	Lab 3: Logic Gates (XOR, XNOR)
Week 4	Lab 4: Exercises
Week 5	Lab 5: Universal Gates (NAND, NOR)
Week 6	Lab 6: Flip-Flop
Week 7	Lab 7: Adder (Half and Full Adder)

Week 8	Lab 8: Subtractor (Half and Full Subtractor)
Week 9	Lab 9: Comparator
Week 10	Lab 10: Asynchronous Binary Counter Up
Week 11	Lab 11: Asynchronous Binary Down Counter
Week 12	Lab 12: Asynchronous Binary Decade Counter
Week 13	Lab 13: Asynchronous MOD Counter
Week 14	Lab 14: Asynchronous Binary Counter (count from number to another)

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	DIGITAL FUNDAMENTALS / FLOYD	YES
Recommended Texts	Digital Logic Design - 4th Edition	NO
Websites	https://www.udemy.com/course/digital-electronics-logic-design/?utm_source=adwords&utm_medium=udemyads&utm_campaign=DSA_Catch all_la.EN_cc.ROW&utm_content=deal4584&utm_term=_._ag_88010211481_._ad_535397282061_._kw__._de_c_._dm__._pl__._ti_dsa-52949608673_._li_1007949_._pd__._&matchtype=&gclid=CjwKCAjwp6CkBhB_EiwAlQVyxcuQ427tsVehXbetXE4NUFlekP4rqq-PrCWgQfIucPuo7Mqz8SXRVxoC5asQAvD_BwE	

Grading Scheme
مخطط الدرجات

Group	Grade	التقدير	Marks (%)	Definition
Success Group (50 - 100)	**A** - Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX** – Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.