وزارة التعليم العالي والبحث العلمي

جهاز الاشراف والتقويم العلمي

دائرة ضمان الجودة والاعتماد الأكاديمي

استمارة وصف البرنامج الأكاديمي للعام الدراسي ٢٠٢٥-٢٠٢٦ للكليات والمعاهد

الجامعة : جامعة شط العرب الاهلية

الكلية \المعهد : الكلية التقنية الهندسية

القسم العلمي : قسم هندسة تقنيات الحاسوب

تاريخ ملء الملف : ٢٠٢٥\٩\١

التوقيع

اسم رئيس القسم : قاسم عبدالجبار رشيد ابراهيم

التاريخ : ١/٩/ ٢٠٢٥

التوقيع

اسم المعاون العلمي : م.م. عصام خليل ابراهيم

التاريخ : /٩/ ٢٠٢٥

م.عصام خليل ابراهيم
معاون العميد للشؤون العلمية

دقق الملف من قبل

شعبة ضمان الجودة والأداء الجامعي

اسم مدير شعبة ضمان الجودة والأداء الجامعي

مصادقة السيد العميد

أ.م.د. مازن عبدالاله علوان
عميد الكلية التقنية الهندسية

MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

Module Information معلومات المادة الدراسية			
Module Title	Digital Systems	Module Delivery	
Module Type	Core	✓ Theory Lecture ✓ Lab Tutorial Practical Seminar	
Module Code	CET1201		
ECTS Credits	6		
SWL (hr/sem)	150		
Module Level	1	Semester of Delivery	2
Administering Department	CET	College	EETC
Module Leader		e-mail	
Module Leader's Acad. Title	Lecturer	Module Leader's Qualification	Msc.
Module Tutor		e-mail	
Peer Reviewer Name		e-mail	
Scientific Committee Approval Date	1/9/2025	Version Number	1.0

Relation with other Modules العلاقة مع المواد الدراسية الأخرى			
Prerequisite module	CET1101	Semester	1
Co-requisites module	None	Semester	

Module Aims, Learning Outcomes and Indicative Contents أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية	
Module Aims أهداف المادة الدراسية	1. To understand the flip flop operation. 2. To understand the latches operation. 3. This course deals with the designing of logic systems. 4. To understand the principles of counter circuits. 5. To understand the shift registers. 6. To have a skill to design ADC and DAC.
Module Learning Outcomes مخرجات التعلم للمادة الدراسية	1. Discuss the flip-flops. 2. Recognize the differences between flip-flops and latches. 3. List the applications of flip-flops. 4. Summarize what is meant by the logic systems. 5. Explain the counter circuits and discuss the difference between synchronous and asynchronous counter. 6. Discuss the types of asynchronous counter circuits. 7. Discuss the types of synchronous circuit. 8. Identify the shift registers. 9. Discuss the operations of each types of shift registers. 10. Discuss the shift register counter. 11. Explain the principles of ADC and DAC. 12. Explain the design for each type of ADC and DAC.
Indicative Contents المحتويات الإرشادية	Indicative content includes the following. --Flip-Flops – SR latch, T latch, D latch. **[10 hrs]** --Flip-Flops- JK FF, edge triggered, and conversion from one type to another. [**10 hrs]** --Counters- Asynchronous, synchronous counters, Decade, up-down counters, and counter decoding. **[15 hrs]** --Shift-registers - serial in/serial out, serial in/parallel out, parallel in/serial out, parallel in/parallel out, bidirectional , shift register counter (Johnson counter, Ring counter)) **[10 hrs]** --Multivibrators- definition, astable, bistable, mono-stable, and 555 timer **[5 hrs]** --A/D convertors modeling -flash ADC, tacking ADC, slope ADC ,successive approximation ADC, digital ramp ADC, delta sigma ADC. **[5 hrs]** --D/A convertors modeling -R/2R DAC, R/2nR DAC. **[5 hrs]**
Learning and Teaching Strategies	

استراتيجيات التعلم والتعليم	
Strategies	Type something like: The main strategy that will be adopted in delivering this module is to encourage students' participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering type of simple experiments involving some sampling activities that are interesting to the students.

Student Workload (SWL) الحمل الدراسي للطالب موزعة على 15 اسبوع			
Structured SWL (h/sem) الحمل الدراسي المنتظم للطالب خلال الفصل	64	**Structured SWL (h/w)** الحمل الدراسي المنتظم للطالب أسبوعيا	4.26
Unstructured SWL (h/sem) الحمل الدراسي غير المنتظم للطالب خلال الفصل	86	**Unstructured SWL (h/w)** الحمل الدراسي غير المنتظم للطالب أسبوعيا	5.73
Total SWL (h/sem) الحمل الدراسي الكلي للطالب خلال الفصل	150		

Module Evaluation تقييم المادة الدراسية					
		Time/Number	**Weight (Marks)**	**Week Due**	**Relevant Learning Outcome**
Formative assessment	**Quizzes**	1	10% (10)	8	LO #1-7
	Assignments	2	10% (10)	4, 10	LO # 1, 3, LO # 3- 8
	Projects / Lab.	10	10% (1)	Continuous	LO # 1-14
	Report	10	10% (1)	Continuous	LO # 1-14
Summative assessment	**Midterm Exam**	2 hr	10% (10)	10	LO # 1-10
	Final Exam	4hr	50% (50)	16	All
Total assessment			100% (100 Marks)		

Delivery Plan (Weekly Syllabus) المنهاج الاسبوعي النظري	
	Material Covered
Week 1	Flip-flops and laches(SR latch, D latch)
Week 2	Flip-Flops(T-latch, JK)
Week 3	Flip-Flops(edge triggered, master-slave)
Week 4	Flip-flops (conversion from one type to another, flip flop applications)
Week 5	Asynchronous counter
Week 6	Synchronous counter
Week 7	Decade, up-down counter
Week 8	Cascade counter, Counter decoding
Week 9	Shift-registers (serial in/serial out, serial in/parallel out, parallel in/serial out, parallel in/parallel out)
Week 10	Midterm exam
Week 11	Shift-registers (bidirectional , shift register counter), Johnson counter, Ring counter
Week 12	Multivibrators (definition, astable, bistable)
Week 13	Multivibrators (monostable, 555 timer)
Week 14	A/D convertors (flash ADC, tacking ADC, slope ADC ,successive approximation ADC, digital ramp ADC, delta sigma ADC)
Week 15	D/A convertors (R/2R DAC, R/2^nR DAC)
Week 16	**Preparatory week before the final Exam**

Delivery Plan (Weekly Lab. Syllabus) المنهاج الاسبوعي للمختبر	
	Material Covered
Week 1	SR ff, T ff
Week 2	D ff, JK ff
Week 3	Master-slave ff
Week 4	asynchronous counter (2-bit,3-bit)

Week 5	asynchronous counter(4-bit, modulus counter)
Week 6	synchronous counter (2-bit, 3-bit)
Week 7	synchronous counter (decade, up-down counter)
Week 8	Cascade counter, counter decoding
Week 9	Serial in-serial out, parallel in-parallel out shift register
Week 10	Serial in-parallel out, parallel in- serial out SR
Week 11	Johnson counter, ring counter
Week 12	multivibrator
Week 13	Analogue to digital convertor
Week 14	Digital to analogue convertor

Learning and Teaching Resources
مصادر التعلم والتدريس

	Text	Available in the Library?
Required Texts	Digital Fundamentals by Floyed	Yes
Recommended Texts	Digital circuit analysis and design with Simulink modeling by Steven T. Karris	No
Websites	https://www.coursera.org/browse/physical-science-and-engineering/electrical-engineering	

Grading Scheme
مخطط الدرجات

Group	Grade	التقدير	Marks (%)	Definition
Success Group (50 - 100)	**A -** Excellent	امتياز	90 - 100	Outstanding Performance
	B - Very Good	جيد جدا	80 - 89	Above average with some errors
	C - Good	جيد	70 - 79	Sound work with notable errors
	D - Satisfactory	متوسط	60 - 69	Fair but with major shortcomings
	E - Sufficient	مقبول	50 - 59	Work meets minimum criteria
Fail Group (0 – 49)	**FX –** Fail	راسب (قيد المعالجة)	(45-49)	More work required but credit awarded
	F – Fail	راسب	(0-44)	Considerable amount of work required

Note: Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above.