MODULE DESCRIPTION FORM

نموذج وصف المادة الدراسية

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| **Module Information****معلومات المادة الدراسية** |
| **Module Title** | Digital Fundamentals | **Module Delivery** |
| **Module Type** | Core | * **✔ Theory**
* **Lecture**
* **✔ Lab**
* **Tutorial**
* **Practical**
* **Seminar**
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| **Module Code** | CET1101 |
| **ECTS Credits**  | 6 |
| **SWL (hr/sem)** | 150 |
| **Module Level** | UGx11 1 | **Semester of Delivery** | 1 |
| **Administering Department** | CET |  **College** |  EETC |
| **Module Leader** | Reem Jamal |  **e-mail** | Reem84j@mtu.edu.iq |
| **Module Leader’s Acad. Title** | lecturer | **Module Leader’s Qualification** | Msc. |
| **Module Tutor** | Raya Majid Hameed |  **e-mail** | Rayamajid89@mtu.edu.iq |
| **Peer Reviewer Name** | Asst. Prof. Alhamzah Taher Mohammed |  **e-mail** | alhamza\_tm@mtu.edu.iq |
| **Scientific Committee Approval Date** | 29/10/2023 | **Version Number** | 1.0 |

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| **Relation with other Modules****العلاقة مع المواد الدراسية الأخرى** |
| **Prerequisite module** | None | **Semester** |  |
| **Co-requisites module** | None | **Semester** |  |

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| **Module Aims, Learning Outcomes and Indicative Contents****أهداف المادة الدراسية ونتائج التعلم والمحتويات الإرشادية** |
|  **Module Aims****أهداف المادة الدراسية** | 1. To be able to deal with the number systems and codes.
2. To understand the functionality of logic gates.
3. To have a skill to use the logic gates in designing logic circuit.
4. To have a skill to simplify the digital circuits.
5. To learn the simplification process, Boolean expression, Demorgans law, and Karnaugh map..
6. To understand the principles for designing logic circuit.
7. To understand adder, subtractor, decoder, incoder, multiplexer, demultipleaer, and comparator circuits.
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| **Module Learning Outcomes****مخرجات التعلم للمادة الدراسية** | 1. Recognize each type of number systems.
2. Identify the process of converting between number systems.
3. Summarize the types of logic gates.
4. Discuss the use of each gate.
5. Describe design of logic circuit by using logic gats.
6. Explain the simplification processes.
7. Explain Boolean expression and Demorgan’s law.
8. Explain the Karnaugh map for different numbers of bits.
9. Discuss the design of logic circuit before and after simplification.
10. Explain the combinational logic circuit.
11. Identify the adder, subtractor, decoder, encoder, multiplexer, demultiplexer, comparator circuits, and code conversion.
12. Identify the basic circuit elements and their applications
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| **Indicative Contents****المحتويات الإرشادية** | Indicative content includes the following.--Number systems - decimal, binary, octal, and hexadecimal number system, conversion, operation. **[8 hrs]**-Codes- excess-3,gray code, conversions, operations, complements **[8 hrs]**--Logic gates-NOT, AND, OR, NOR, NAND, XOR, XNOR. **[5 hrs]**--Logic simplification-Boolean theorem and Demorgans law. **[10 hrs]**--Karnaugh map-SOP, POS, and don’t care. **[10 hrs]**--Arithmetic operations Part A- adder, parallel binary adder, subtractor, adder-subtractor. **[10 hrs]** --Arithmetic operations Part B- multiplexer, demultiplexer, decoder, encoder, comparator, and code conversion. **[10 hrs]** |

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| **Learning and Teaching Strategies****استراتيجيات التعلم والتعليم** |
| **Strategies** | Type something like: The main strategy that will be adopted in delivering this module is to encourage students’ participation in the exercises, while at the same time refining and expanding their critical thinking skills. This will be achieved through classes, interactive tutorials and by considering type of simple experiments involving some sampling activities that are interesting to the students. |

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| **Student Workload (SWL)****الحمل الدراسي للطالب موزع على 15 اسبوع** |
| **Structured SWL (h/sem)****الحمل الدراسي المنتظم للطالب خلال الفصل** | 64 | **Structured SWL (h/w)****الحمل الدراسي المنتظم للطالب أسبوعيا** | 4.26 |
| **Unstructured SWL (h/sem)****الحمل الدراسي غير المنتظم للطالب خلال الفصل** | 86 | **Unstructured SWL (h/w)****الحمل الدراسي غير المنتظم للطالب أسبوعيا** | 5.73 |
| **Total SWL (h/sem)****الحمل الدراسي الكلي للطالب خلال الفصل** | 150 |

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| **Module Evaluation****تقييم المادة الدراسية** |
| **As** | **Time/Number** | **Weight (Marks)** | **Week Due** | **Relevant Learning Outcome** |
| **Formative assessment** | **Quiz** | 2 | 10% (10) | 5, 10 | LO #1- 3, LO # 4 - 8 |
| **Assignments** | 1 | 10% (10) | 12 | LO # 1-11  |
| **Projects / Lab.** | 1 | 10% (10) | Continuous | LO # 1-12 |
| **Report** | 1 | 10% (10) | Continuous | LO # 1-12 |
| **Summative assessment** | **Midterm Exam** | 2 hr | 10% (10) | 10 | LO # 1-10 |
| **Final Exam** | 4hr | 50% (50) | 16 | All |
| **Total assessment** | 100% (100 Marks) |  |  |

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| **Delivery Plan (Weekly Syllabus)****المنهاج الاسبوعي النظري** |
| **Week**  | **Material Covered** |
| **Week 1** | Number systems (decimal, binary, octal, conversions, operations) |
| **Week 2** | Number systems (hexadecimal, BCD, conversions, operations) |
| **Week 3** | Number systems (excess-3,gray code, conversions, operations, complements) |
| **Week 4** | Logic gates (AND,OR,NOT,NAND,NOR,XOR,XNOR) |
| **Week 5** | Logic simplification (Boolean theorem) |
| **Week 6** | Logic simplification (Demorgan’s theorem) |
| **Week 7** | Karnaugh maps( 2-variables,3-variables,) |
| **Week 8** | Karnaugh maps (4-variables (SOP,POS,don’t care)) |
| **Week 9** | Karnaugh maps (5-variables, (SOP,POS,don’t care)) |
| **Week 10** | Midterm exam |
| **Week 11** | Arithmetic operations  |
| **Week 12** | Arithmetic operations (decoder, encoder) |
| **Week 13** | Arithmetic operations (Multiplexer, Demultiplexer) |
| **Week 14** | Arithmetic operations (comparators)  |
| **Week 15** | Arithmetic operations (code conversion) |
| **Week 16** | **Preparatory week before the final Exam** |

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| **Delivery Plan (Weekly Lab. Syllabus)****المنهاج الاسبوعي للمختبر** |
| **Week**  | **Material Covered** |
| **Week 1** | logic gates (NOT, AND,OR) |
| **Week 2** |  Logic gates (NOR.NAND) |
| **Week 3** | Logic gates (XOR,XNOR) |
| **Week 4** | Boolean theorem |
| **Week 5** | Demorgan’s law |
| **Week 6** | Karnaugh map  |
| **Week 7** | SOP |
| **Week 8** |  POS, don’t care |
| **Week 9** | Combinational circuit (half adder, full adder) |
| **Week 10** | Combinational circuit (Half subtractor, full subtractor) |
| **Week 11** | Decoder and Encoder circuits |
| **Week 12** | Multiplexer and Demultiplexer circuits |
| **Week 13** | Comparator circuit |
| **Week 14** | Code conversion circuits |

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| **Learning and Teaching Resources****مصادر التعلم والتدريس** |
|  | **Text** | **Available in the Library?** |
| **Required Texts** | Digital Fundamentals by Floyed | Yes |
| **Recommended Texts** | Digital circuit analysis and design with Simulink modeling by Steven T. Karris | No |
| **Websites** |  |

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|  **Grading Scheme****مخطط الدرجات** |
| **Group** | **Grade** | التقدير | **Marks (%)** | **Definition** |
| **Success Group****(50 - 100)** | **A -** Excellent | **امتياز** | 90 - 100 | Outstanding Performance |
| **B -** Very Good | **جيد جدا**  | 80 - 89 | Above average with some errors |
| **C -** Good | **جيد** | 70 - 79 | Sound work with notable errors |
| **D -** Satisfactory | **متوسط**  | 60 - 69 | Fair but with major shortcomings |
| **E -** Sufficient | **مقبول**  | 50 - 59 | Work meets minimum criteria |
| **Fail Group****(0 – 49)** | **FX –** Fail | **راسب (قيد المعالجة)** | (45-49) | More work required but credit awarded |
| **F –** Fail | **راسب** | (0-44) | Considerable amount of work required |
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| **Note:** Marks Decimal places above or below 0.5 will be rounded to the higher or lower full mark (for example a mark of 54.5 will be rounded to 55, whereas a mark of 54.4 will be rounded to 54. The University has a policy NOT to condone "near-pass fails" so the only adjustment to marks awarded by the original marker(s) will be the automatic rounding outlined above. |