



### Course Weekly Outline

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<b>Subject Name</b>	Microprocessor architecture				
<b>Course Objective</b>	<p>1- Knowledge of the basic parts of a computer and the types of microprocessors.</p> <p>2- Knowing the main and secondary types of memory in the computer.</p> <p>3- Know the components of the CPU in the computer.</p> <p>4- Possess the ability to program microprocessors.</p>				
<b>Course Description</b>	<p>Understand the infrastructure of a central unit.</p> <p>Knowing how to transfer data through the rules inside the computer.</p> <p>Knowledge of the types of microprocessors in the form of differences in microprocessors (8086 and .8085) in particular.</p>				
<b>References</b>	<p>1- Digital Fundamental by Floyed.</p> <p>2-Ramesh S. Goankar, “Microprocessor Architecture, Programming and Applications with 8085”, 5thEdition, Prentice Hall.</p>				
<b>Course Assessment</b>	<b>Term Exam</b>	<b>Project</b>	<b>laboratory</b>	<b>Quizzes and Attendance</b>	<b>Final Exam</b>
	20	-	10	10	60



Objectives	Scientific material	Theoretical material	date	week
<p>1- Know the history and evolution of the stages of the computer. 2- Knowing the basic structure of the main and secondary memory. 3- Understand the basic structure of the CPU. 4- The ability to carry out the instructions of the Microprocessor. The ability to carry out the instructions of the Microprocessor.</p>	General architecture of digital computer, review of 8085	General architecture of digital computer, review of 8085	4/10/2022	1,2
	8085 memory Addressing	8085 memory Addressing	11/10/2022	3,4
	8085 1/0 Addressing	8085 1/0 Addressing	18/10/2022	5,6
	8085 machine cycle & bus timing	8085 machine cycle & bus timing	25/9/2022	7
	8085 Interrupt Types	8085 Interrupt Types	1/11/2022	8,9
	Introduction to 8086	Introduction to 8086	8/11/2022 15/11/2022	10
	Software Architecture, BIU, EU, registers, pipeline	Software Architecture, BIU, EU, registers, pipeline	22/11/2022 29/11/2022	11, 12
	Memory segmentation, generating memory address	Memory segmentation, generating memory address	6/12/2022	13
	Hardware organization space, Data 8086 ( Organization aligned and misaligned word, double word)	Hardware organization space, Data 8086 ( Organization aligned and misaligned word, double word)	21/2/2023	14
Pin configuration, min &max mode,8288 bus controller, 8284 system clock	Pin configuration, min &max mode,8288 bus controller, 8284 system clock	28/2/2023 7/3/2023	15, 16	

	Addressing mode, machine language coding	Addressing mode, machine language coding	14/3/2023 21/3/2023	17, 18
	8086 instructions set	8086 instructions set	28/3/2023 4/4/2023	19- 23
	Stack memory, POP & PUSH instructions	Stack memory, POP & PUSH instructions	11/4/2023	24
	Memory read & write Bus Cycles, Idle & wait state	Memory read & write Bus Cycles, Idle & wait state	18/4/2023	25
	Memory Interface Circuits, bus transceivers, Bank Write and Bank Read Control Logic, memory expansion.	Memory Interface Circuits, bus transceivers, Bank Write and Bank Read Control Logic, memory expansion.	25/4/2023 2/5/2023	26, 27
	1/0 Interface Circuits (Isolated input/output & Memory input/output, 1/0 instructions,	1/0 Interface Circuits (Isolated input/output & Memory input/output, 1/0 instructions,	9/5/2023 16/5/2023	28, 29
	8086 Interrupt Types	8086 Interrupt Types	23/5/2023	30

**Lecturer signature**

**Head of Department Signature**