The Republic of Iraq
Ministry of Higher Education and Scientific Research
Scientific Supervision and Evaluation Authority

University: Shatt Al-Arab University
College: College of technical Engineering

Department Laser and Optoelectronics Engineering Technology
The First stage
Lecturer Name: Dr. Murtadha Muayad Naeem
Academic qualification: PhD
Place of work: Shatt Al-Arab University

weekly lesson schedule

Course Lecturer	**Dr. Murtadha Muayad Naeem**
e-mail	
Title	Digital Fundamentals and Logics
Course Coordinator	
Course Objectives	This comprehensive course provides a basic understanding of the principles of Digital Logic. This course aims to enable the student to: 1. Explain the number systems. 2. Perform arithmetic operations on binary number systems. 3. Define the logic gates. 4. Write the logic expression of the logic circuits. 5. Produce the truth table for the logic expressions. 6. Simplify the Boolean expressions. 7. Understand the functions of combinational logic circuits. 8. Analyze and design various combinational logic circuits.
Course Description	- Understand number systems and convert values between decimal, binary, octal, and hexadecimal representations. - Explain the principles of binary arithmetic, including addition, subtraction, and the use of 1's and 2's complements. - Identify and describe the function of basic logic gates using symbols, truth tables, and Boolean expressions. - Apply Boolean algebra laws and theorems to simplify logic expressions. - Analyze logic circuits to derive Boolean expressions and corresponding truth tables. - Use Karnaugh maps to minimize logic expressions in both SOP and POS forms. - Design and implement basic combinational logic circuits such as adders, subtractors, comparators, and code converters. -Evaluate different circuit designs for efficiency and simplicity using universal gates..
Textbooks	1. G. K. Kharate, "Digital Electronics" Oxford university press, 7th edition, ISBN 13: 978-0-19-806183-0, 2013. 2. Thomas L. Floyd, "Digital Fundamentals" Pearson Education, 11th edition, ISBN 10: 1-292-07598-8, 2015.

	3. T. Ndjountche “Digital Electronics 1”, John Wiley & Sons, 1st edition, ISBN 978-1-84821-984-7, 2016. 4. N. S. Widmer, G. L. Moss, R. J. Tocci, “Digital Systems”, Pearson Education Limited e, 12th edition, ISBN 978-0-134-22013-0, 2017. 5. Shuqin Lou, Chunling Yang, “Digital Electronic Circuits” Science Press, 4th edition, ISBN 978-3-11-061466-4, 2019.

final exam 50	project	Assignment	daily exams	lab	Midterm Exam
	10	10	10	10	10

General Notes		

The Republic of Iraq
Ministry of Higher Education and Scientific Research
Scientific Supervision and Evaluation Authority

University: Shatt Al-Arab
College: College of technical Engineerin
Department Laser and Optoelectronics Engineering Technology
The First stage
Lecturer Name: Alaa Naser Khraibet
..Scientific title:
Academic qualification:
Place of work: Shatt Al-Arab University

weekly lesson schedule

Week	Date	Topics Covered	Number of Hours	Notes
١		Introduction - Number Systems: binary, decimal, octal, and hexadecimal numbers.		
٢		Convert a decimal number to any radix number.		
٣		Convert a binary number to an octal or hexadecimal number and vice versa, and convert an octal number to a hexadecimal number and vice versa.		
٤		Perform arithmetic operations on binary numbers,and convert a binary number to its 1's complement, and 2's complement.		
٥		Identify the logic gates, write the logic expression, and produce the truth table.		
٧-٦		Analyze a combinational logic circuit, draw a logic diagram, and theorems of Boolean algebra. DE Morgan's theorem, standard SOP expression, and standard POS expression.		
٩-٨		Mid-term Exam + Construct a Karnaugh map for two, three, and four variables, use a Karnaugh map to minimize POS & SOP expressions. Convert nonstandard expressions to standard expressions, and Use the Karnaugh map to convert between POS and SOP.		
١٢-١١-١٠		Use NAND gates to create other logic gates, Use NOR gates to create other logic gates, and implement the logic functions using only NAND gates or only NOR gates. Design half-adder & full-adder logic circuits, and use full-adders to implement a parallel binary adder. Design the half- subtractor & full-subtractor logic circuits, and use full-subtractors to implement a parallel binary subtractor.		
١٤-١٣		Explain the concept of code converters, and describe gray code, BCD, and excess-3 code. Design combinational logic circuits that convert		

		from one coding method to another.		
١٥		Design 1-bit, and 2-bit comparators using logic gates, and use the 74HC85 comparator to compare the magnitudes of two 4-bit numbers.		

The Republic of Iraq
Ministry of Higher Education and Scientific Research
Scientific Supervision and Evaluation Authority

University: Shatt Al-Arab
College: College of technical Engineerin
Department Laser and Optoelectronics Engineering Technology
The First stage
Lecturer Name: Alaa Naser Khraibet
..Scientific title:
Academic qualification:
Place of work: Shatt Al-Arab University

Weekly Lesson Plan (Lab)

Week	Number of hours	Topics covered
١-٢		Explain the function of a logic gates (AND, OR, NOT, AND, NOR, XOR , and XNOR) using the logical board. Implement the logic gates (AND, OR, & NOT) using diodes, transistors, and resistors.
٣-٤		Verify the truth table of logic gates (AND, OR, NOT, NAND, NOR, XOR, &XNOR) by using integrated circuits IC (7408, 7432, 7404, 7400, 7402, & 7486). Boolean's algebraic
٥-٦		DE Morgan’s theorem. Implement logic gates (AND, OR, NOT, NAND, NOR, XOR & XNOR) using NAND gates only.
٧-٨		Implement logic gates (AND, OR, NOT, NAND, NOR, XOR & XNOR) using NOR gates only. Design the half-adder circuit using logic gates.
٩-١٠		Design the full-adder circuit using logic gates. Design the half-subtractor circuit using logic gates.
١١-١٢		Design the full-subtractor circuit using logic gates. Design the full subtractor circuit using logic gates.
١٤-١٣		Implement a binary to gray code converter circuit using logic gates. Implement the BCD to Excess-3 code converter circuit using logic gates.
١٥		Design (1-bit) comparator circuit using logic gates.

Lecturer’s signature: **Head of Department’s signature:**